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Design and Control for the Buck-Boost Converter Combining 1-Plus-D Converter and Synchronous Rectified Buck Converters

Jeevan Naik
Project Engineer, CSIR - National Aerospace Laboratories, Bangalore – 560 017, India

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ABSTRACT

In this paper, a design and control for the buck-boost converter, i.e., 1-plus-D converter with a positive output voltage, is presented, which combines the 1-plus-D converter and the synchronous rectified (SR) buck converter. By doing so, the problem in voltage bucking of the 1-plus-D converter can be solved, thereby increasing the application capability of the 1-plus-D converter. Since such a converter operates in continuous conduction mode inherently, it possesses the nonpulsating output current, thereby not only decreasing the current stress on the output capacitor but also reducing the output voltage ripple. Above all, both the 1-plus-D converter and the SR buck converter, combined into a buck–boost converter with no right-half plane zero, use the same power switches, thereby causing the required circuit to be compact and the corresponding cost to be down. Furthermore, during the magnetization period, the input voltage of the 1-plus-D converter comes from the input voltage source, whereas during the demagnetization period, the input voltage of the 1-plus-D converter comes from the output voltage of the SR buck converter.

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Corresponding Author:

Jeevan Naik
Project Engineer,
CSIR - National Aerospace Laboratories,
Bangalore – 560 017, India.
Email: jeevannaik@hotmail.com

1. INTRODUCTION

As generally recognized, many applications require voltage-bucking/boosting converters, such as portable devices, car electronic devices, etc. This is because the battery has quite large variations in output voltage, and hence, the additional switching power supply is indispensable for processing the varied input voltage so as to generate the stabilized output voltage. There are several types of nonisolated voltage buck/boosting converter [1]–[9], such as buck–boost converter, single-ended primary-inductor converter (SEPIC), Cuk converter, Zeta converter, Luo converter and its derivatives, etc. However, these converters, operating in the continuous conduction mode (CCM), possess right-half plane zeros, thus causing system stability to be low. Consequently, a KY buck–boost converter [10] has been presented to conquer the aforementioned problems, but it has a serious problem in four power switches used, thereby causing the corresponding cost to be up.

In order to reduce the number of power switches in [10], the 1-plus-D converter and the SR buck converter, combined into a buck–boost converter, both use the same power switches. Aside from this, the proposed converter has no right-half plane zero due to the input connected to the output during the turn-on period, and this converter always operates in CCM due to the positive and negative inductor currents existing at light load simultaneously. As compared with the converters previously stated, this converter has the nonpulsating output inductor current, thereby causing the current stress on the output capacitor to be

decreased, and hence, the corresponding output voltage ripple to be small. Moreover, such a converter has the positive output voltage different from the negative output voltage of the buck–boost converter. In this paper, the detailed illustration of the operation of this converter is given, along with some simulated results provided to verify the effectiveness of the proposed topology.

Prior to the end of this section, there is a comparison between the converters presented in [11] and the proposed converter. Since the proposed converter is used to buck/boost voltage, the voltage boosting range is not so high, that is, the voltages across two energy-transferring capacitors C1 and C2 are both D times the input voltage, where D is the duty cycle of the gate driving signal for the main switch. Regarding the converters shown in [11], the voltages across two energy-transferring capacitors C1a and C1b for the hybrid Cuk converter, the hybrid Zeta converter, and the hybrid SEPIC converter are 1/(1−D), D/(1−D), and 1/(1−D) times the input voltage, respectively. Therefore, the converters shown in [11] have higher voltage conversion ratios than that of the proposed converter. Therefore, from an industrial point of view, the converters shown in [11] are suitable for sustainable energy applications, whereas the proposed converter is suitable for portable products.

Furthermore, since the proposed converter comes from the 1-plus-D converter, the detailed comparisons between the proposed buck–boost converter and the 1-plus-D converter are described as follows.

1) Both converters always operate in CCM. That is, the negative current can be allowed at light load, but the corresponding average current must be positive.
2) Both converters have individual output inductors, thereby causing the output currents to be nonpulsating.
3) The proposed converter has one additional inductor and one additional capacitor so as to execute voltage bucking/boosting as compared with the 1-plus-D converter. The maximum voltage conversion ratios for both are identical, equal to 2. Both these converters can operate bidirectional.
4) The proposed converter works with the backward voltage conversion ratio of 0.5/ (1-D), whereas the 1-plus-D converter works with the backward voltage conversion ratio of 1/ (2-D).

2. PROPOSED CONVERTER STRUCTURE

Figure 1 shows a proposed buck–boost converter, which combines two converters using the same power switches. One is the SR buck converter, which is built up by two power switches S_1 and S_2, one inductor L_1, one energy-transferring capacitor C_1, whereas the other is the 1-plus-D converter, which is constructed by two power switches S_1 and S_2, one power diode D_1 which is disconnected from the input voltage source and connected to the output of the SR buck converter, one energy-transferring capacitor C_2, one output inductor L_2, and one output capacitor C_0. The output load is signified by R_0. Furthermore, during the magnetization period, the input voltage of the 1-plus-D converter comes from the input voltage source, whereas during the demagnetization period, the input voltage of the 1-plus-D converter comes from the output voltage of the SR buck converter.

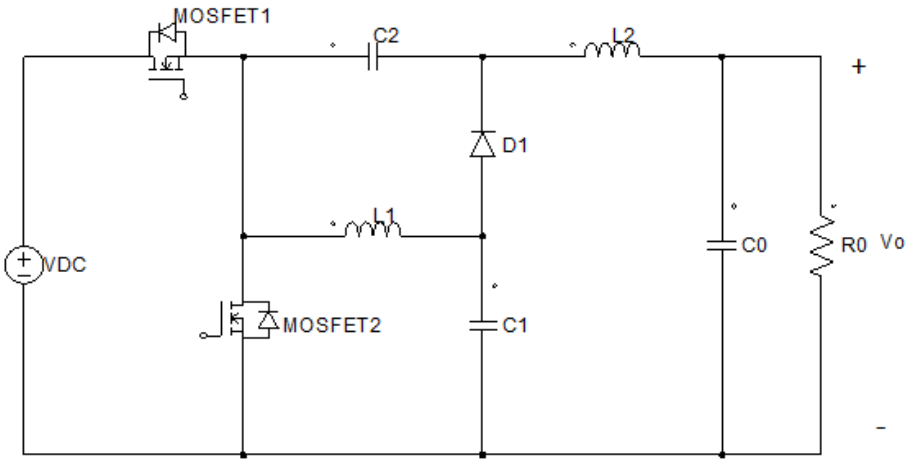


Figure 1. Proposed buck–boost converter

In addition, during the startup period with S_1 being ON and S_2 being OFF, L_1 and L_2 are both magnetized. At the same time, C_1 is charged, and hence, the voltage across C_1 is positive, whereas C_2 is reversing charged, and hence, the voltage across C_2 is negative. Sequentially, during the startup period with S_1 being OFF and S_2 being ON, L_1 and L_2 are both demagnetized. At the same time, C_1 is discharged. Since C_2 is connected in parallel with C_1, C_2 is reverse charged with the voltage across C_2 being from negative to positive, and finally, the voltage across C_2 is the same as the voltage across C_1. After this time onward, the working behavior of this converter will follow the timing sequence shown in Figure 2.

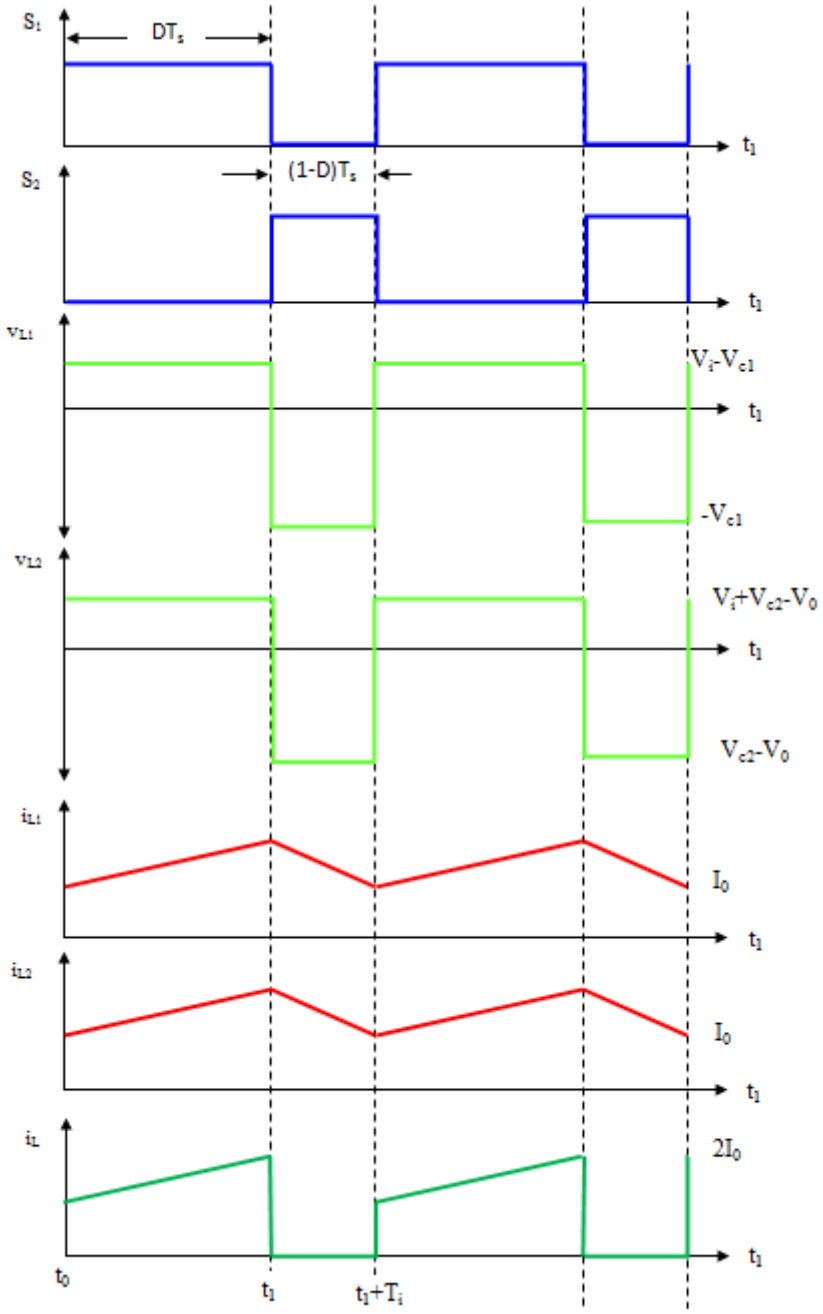


Figure 2. Key waveforms of the proposed converter

3. BASIC OPERATING PRINCIPLES

Before this section is taken up, there are some assumptions are given as follows: 1) all the components are ideal; 2) the blanking times between S_1 and S_2 are omitted; 3) the voltage drops across the switches and diode during the turn-on period are negligible; 4) the values of C_1 and C_2 are large enough to keep V_{C1} and V_{C2} almost constant, that is, variations in V_{C1} and V_{C1} are quite small during the charging and discharging period; 5) the dc input voltage is signified by V_i, the dc output voltage is represented by V_0, the dc output current is expressed by I_0, the gate driving signals for S_1 and S_2 are indicated by M_1 and M_2, respectively, the voltages on L_1 and L_2 are denoted by v_{L1} and v_{L2}, respectively, the currents in L_1 and L_2 are signified by i_{L1} and i_{L2}, respectively, and the input current is expressed by ii; and 6) the currents flowing through L_1 and L_2 are both positive.

Since this converter always operates in CCM inherently, the turn-on type is (D, 1−D), where D is the duty cycle of the gate driving signal for S_1 and 1−D is the duty cycle of the gate driving signal for S_2. Figure 2 shows the key waveforms of the proposed converter with a switching period of Ts under i_{L1} and i_{L2} being positive for any time. It is noted that the input current waveform is pulsating.

4. OPERATING STATES

There are two operating states to be described

State 1:

As shown in Figure 3, S_1 is turned ON but S_2 is turned OFF. During this state, the input voltage provides energy for L_1 and C_1. Hence, the voltage across L_1 is V_i minus V_{C1}, thereby causing L_1 to be magnetized and C_1 is charged.

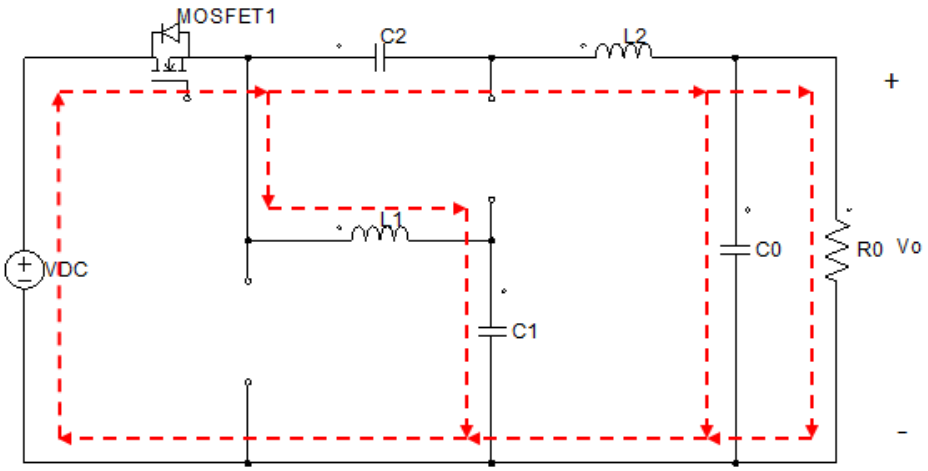


Figure 3. Current flow in state 1

At the same time, the input voltage, together with C_2, provides the energy for L_2 and the output. Hence, the voltage across L_2 is V_i plus V_{C2} minus V_0, thereby causing L_2 to be magnetized, and C_2 is discharged. Therefore, the related equations are depicted as follows:

$$v_{L1} = V_i - V_{c1} \quad (1)$$

$$v_{L2} = V_i + V_{c2} - V_0 \quad (2)$$

State 2:

As shown in Figure 4, S_1 is turned OFF but S_2 is turned ON. During this state, the energy stored in L_1 and C_1 is released to C_2 and the output via L_2. Hence, the voltage across L_1 is minus V_{C1}, thereby causing L_1 to be demagnetized and C_1 is discharged. At the same time, the voltage across L_2 is V_{C2} minus V_0, thereby causing L_2 to be demagnetized and C_2 is charged. Therefore, the associated equations are described as follows:

$$v_{L1} = -V_{c1} \quad (3)$$
$$v_{L2} = V_{c2} - V_0 \quad (4)$$

$$V_{c2} = V_{c1} \quad (5)$$

By applying the voltage-second balance to (1) and (3), the following equation can be obtained as

$$(V_i - V_{c1}) * D * T_s + (-V_{c1}) * (1 - D) * T_s = 0 \quad (6)$$

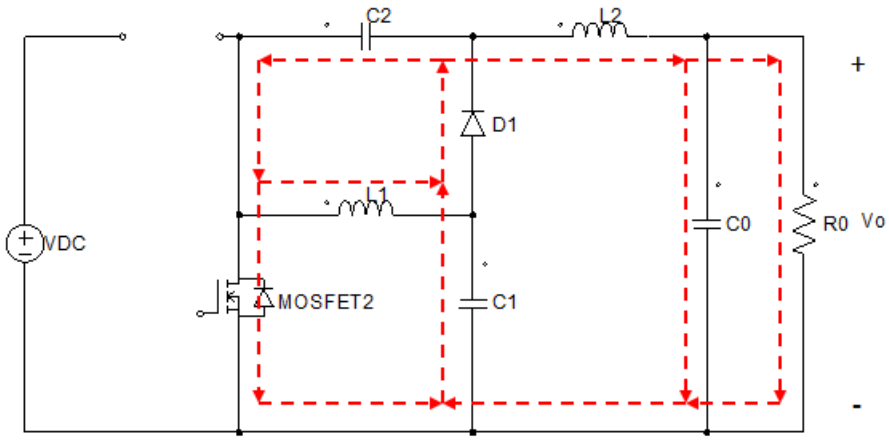


Figure 4. Current flow in state 2

Therefore, by simplifying (6), the following equation can be obtained as

$$V_i * D * T_s - D * V_{c1} * T_s - V_{c1} * T_s + D * V_{c1} * T_s = 0$$
$$V_i * D * T_s - V_{c1} * T_s = 0$$
$$V_i * D * T_s = V_{c1} * T_s$$
$$V_{c1} = D * V_i \quad (7)$$

Sequentially, by applying the voltage-second balance to (2) and (4), the following equation can be obtained as

$$(V_i + V_{c2} - V_0) * D * T_s + (V_{c2} - V_0) * (1 - D) * T_s = 0 \quad (8)$$

Hence, by substituting (5) and (7) into (8), the voltage conversion ratio of the proposed converter can be obtained as

$$V_i * D * T_s + V_{c2} * D * T_s - V_0 * D * T_s + (V_{c2} - V_0) * (1 - D) * T_s = 0$$
$$V_i * D * T_s + V_{c2} * D * T_s - V_0 * D * T_s + V_{c2} * T_s - V_{c2} * D * T_s - V_0 * T_s + V_0 * D * T_s = 0$$
$$V_i * D * T_s + V_{c2} * T_s - V_0 * T_s = 0$$
$$V_i * D * T_s + V_{c2} * T_s = V_0 * T_s$$
$$T_s(V_i * D + V_{c2}) = V_0 * T_s$$
$$V_i * D + V_{c2} = V_0$$

Using equation (5) and (7), the following equation can be obtained as

$$V_i * D + V_{c1} = V_0$$
$$V_i * D + D * V_i = V_0$$
$$2 * V_i * D = V_0$$
$$\frac{V_0}{V_i} = 2 * D \quad (9)$$

Therefore, such a converter can operate in the buck mode as the duty cycle D is smaller than 0.5, whereas it can operate in the boost mode as D is larger than 0.5.

In addition, based on (5), (7), and (9), the dc voltages across C1 and C2 can be expressed to be

$$V_{c1} = V_{c2} = D * V_i$$
$$V_{c1} = V_{c2} = D * \frac{V_0}{(2 * D)}$$
$$V_{c1} = V_{c2} = 0.5V_0 \quad (10)$$

5. DESIGN CALCULATION

In this section, the design of inductors and capacitors are mainly taken into account. Before this section is taken up, there are some specifications to be given as follows: 1) the dc input voltage Vi is from 10V to 16V; 2) the dc output voltage V_0 is 12V; 3) the rated dc load current I_0 rated is 3A; 4) the switching frequency fs is 200 kHz; and 5) the name of S1 and S2 is MOSFET and diode D.

5.1. Inductor Deisgn

From an experimental point of view, the inductor is designed under the condition that no negative current in the inductor exists above 25% of the rated dc load current. Therefore, in this letter, the critical point between positive current and negative current in the inductor is assumed at 25% of the rated dc load current. Therefore, the peak-to-peak values of i_{L1} and i_{L2} are expressed by Δi_{L1} and Δi_{L2}, respectively, and can be obtained according to the following equation:

$$\Delta i_{L1} = \Delta i_{L2} = 0.5\ I_{0\ rated} \quad (11)$$
$$\Delta i_{L1} = \Delta i_{L2} = 0.5 * 3$$

Therefore, Δi_{L1} and Δi_{L2} are 1.5A.

Since the high input voltage makes the inductor not easier to escape from the negative current than the low input voltage, the inductor design is mainly determined by the high input voltage, namely, 16V. Hence, the corresponding minimum duty cycle D_{min} is 0.375. Moreover, based on (10), V_{C1} and V_{C2} are both $0.5V_0$, namely, 6V. Also, the values of L_1 and L_2 can be obtained according to the following equations:

$$L_1 \geq \frac{D_{min} * (V_i - V_{c1})}{\Delta i_{L1} * f_s} \quad (12)$$
$$L_1 \geq \frac{0.375 * (16 - 6)}{1.5 * 200k}$$
$$L_1 \geq 15\mu H$$

Similarly, L_2

$$L_2 \geq \frac{D_{min} * (V_i + V_{c2} - V_0)}{\Delta i_{L2} * f_s} \quad (13)$$
$$L_2 \geq \frac{0.375 * (16 + 6 - 12)}{1.5 * 200k}$$
$$L_1 \geq 15\mu H$$

Therefore, the values of L_1 and L_2 both are calculated to be not less than 12μH, here we used 14μH.

5.2. Capacitor Deisgn

1. Output Capacitor Design

Prior to designing C_o, it is assumed that the output voltage ripple Δv_o is smaller than 1% of the dc output voltage, that is, Δv_o is smaller than 120 mV. Hence, the equivalent series resistance of the output capacitor ESR can be represented by

$$ESR \leq \frac{\Delta v_o}{\Delta i_{L2}} \quad (14)$$
$$ESR \leq \frac{120m}{1.5}$$

$$ESR \leq 80m$$

Accordingly, ESR is calculated to be smaller than 40mΩ, and eventually, one Nippon Chemi-Con (NCC) 1-plus-D series capacitor of 370μF with ESR equal to 36mΩ is chosen for C_0.

2. Energy-Transferring Capacitor Design

Prior to designing the energy-transferring capacitors C_1 and C_2, it is assumed that the values of C_1 and C_2 are large enough to keep V_{C1} and V_{C2} almost at 6V, and hence, variations in V_{C1} and V_{C2} are quite small and are defined to beΔV_{C1} and ΔV_{C2}, respectively. Based on this assumption, ΔV_{C1} and ΔV_{C2} are both set to smaller than 1% of V_{C1} and V_{C2} , respectively, namely, both are smaller than 60mV. Also, in State 1, C_1 is charged whereas C_2 is discharged. Therefore, the values of C_1 and C_2 must satisfy the following equations:

$$C_1 \geq \frac{I_{O-rated} * D_{max}}{\Delta V_{c1} * f_s} \quad (15)$$

$$C_2 \geq \frac{I_{O-rated} * D_{max}}{\Delta V_{c2} * f_s} \quad (16)$$

$$\therefore \quad C_1 \geq \frac{3 * 0.6}{60m * 200k}$$

$$C_1 \geq 150\mu F$$

Similarly

$$C_2 \geq \frac{3 * 0.6}{60m * 200k}$$

$$C_2 \geq 150\mu F$$

Since the maximum duty cycle D_{max} occurs at the input voltage of 10V, namely, 0.6, both the values of C_1 and C_2 are not less than 150μF. Finally, C_1 and C_2 have individual Nippon Chemi-Con 1-plus-D series capacitors of 470μF.

6. CONTROL DESIGN

The aim of the feedback control circuit is to regulate the output voltage v_0. This voltage is compared with the reference value V_0, and the resulting error is feed to PI controller output of the PI signal compared to a triangle signal using a comparator, as illustrated in Figure 5.

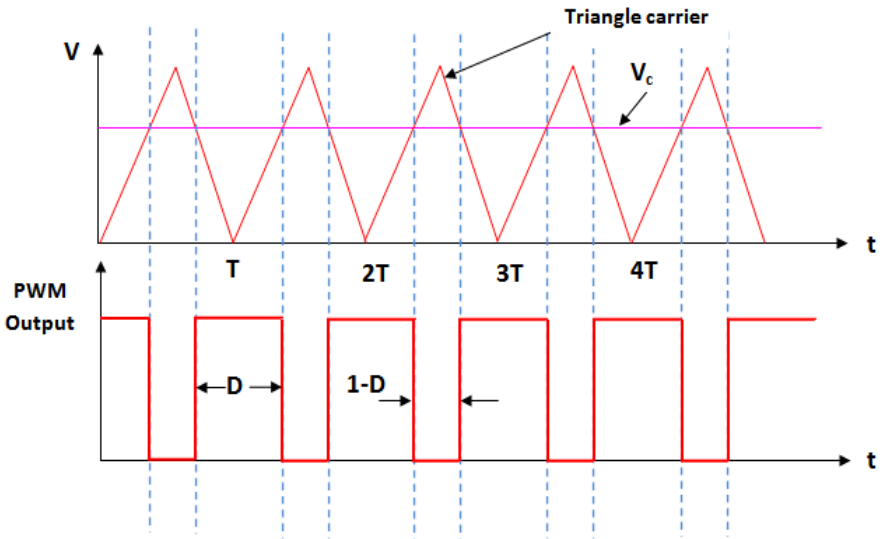
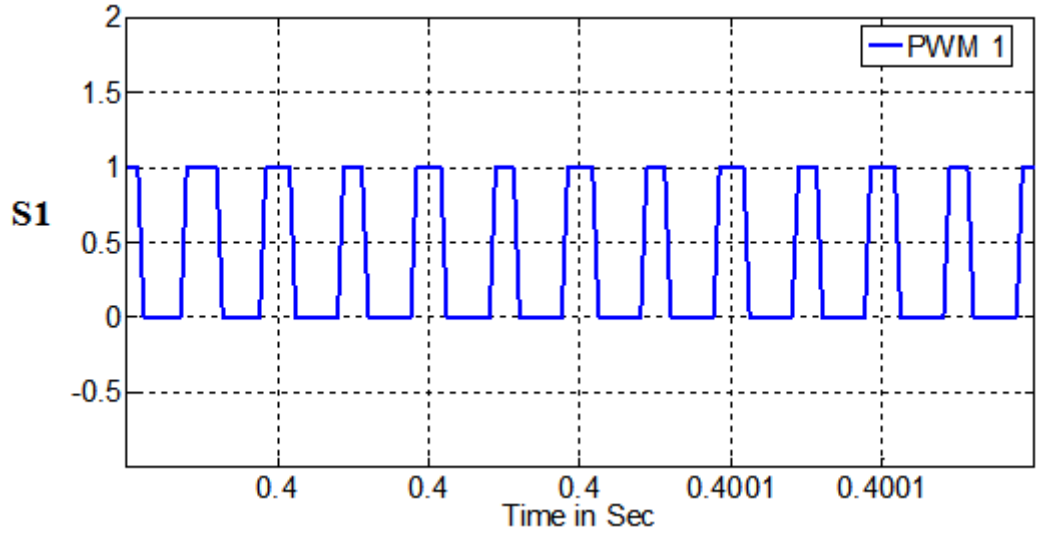


Figure 5. Generation of the switches gate signals

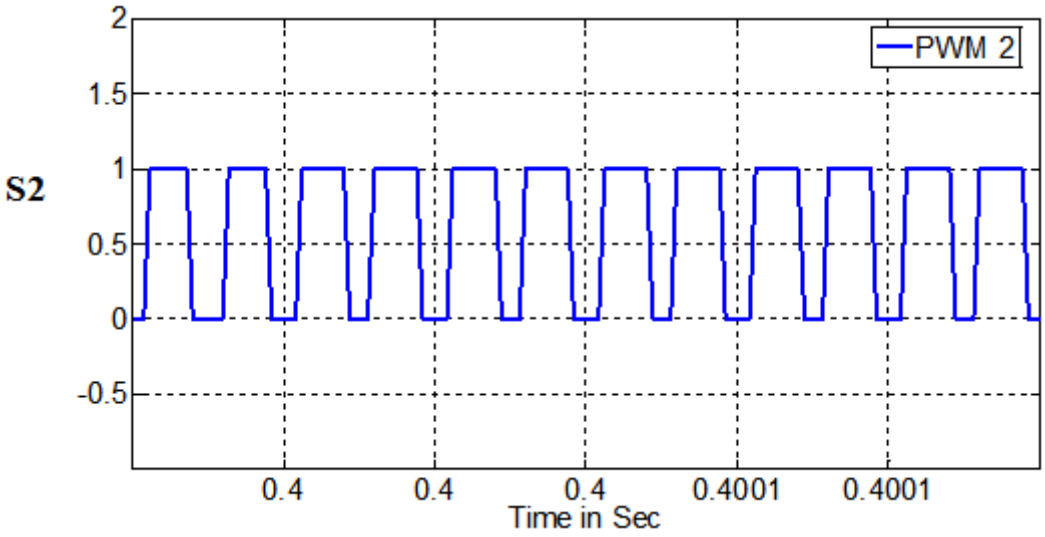
there are three steps to online tune the parameters of the voltage controller to be described in the following. Step 1: the proportional gain kp is tuned from zero to the value which makes the output voltage very close to about 80% of the prescribed output voltage. Step 2: after this, the integral gain ki is tuned from zero to the value which makes the output voltage very close to the prescribed output voltage but somewhat oscillate. Then, ki will be reduced to some value without oscillation. Step 3: from this time onward, the differential gain kd is tuned from zero to the value which accelerates the dynamic response but somewhat oscillate. Then, kd will be reduced to some value without oscillation.

7. EXPERIMENTAL RESULTS

Figure 6 (a) and (b) shows the gate driving signals S1 and S2 for MOSFET1 and MOSFET2. The PWM gate signal generated from PIPWM controlling technique it's reduced the system output error and gives accurate response and better efficiency. Both gate signals are opposite to each other as shown in Figure 6.



(a)



(b)

Figure 6. PWM gate signals (a) PWM 1(b) PWM 2

The wavefroms of the system input voltage shown in Figure 7. In this figure 0 to 0.4 sec the input voltage is 16Volt and 0.4 to 0.6sec voltage is 10Volt. Figure 8 shows the system constant output voltage 12Volt during 0 to 0.4 sec input voltage is 16volt the system is start bucking and during 0.4 to 0.8 sec the system starts boosting and shown in above figure.

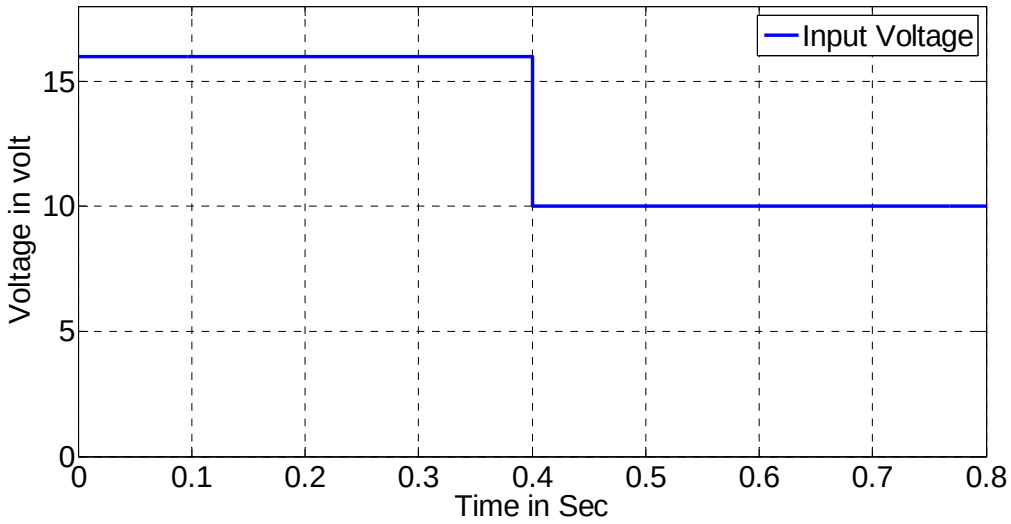


Figure 7. System Input voltage of 10V and 16V

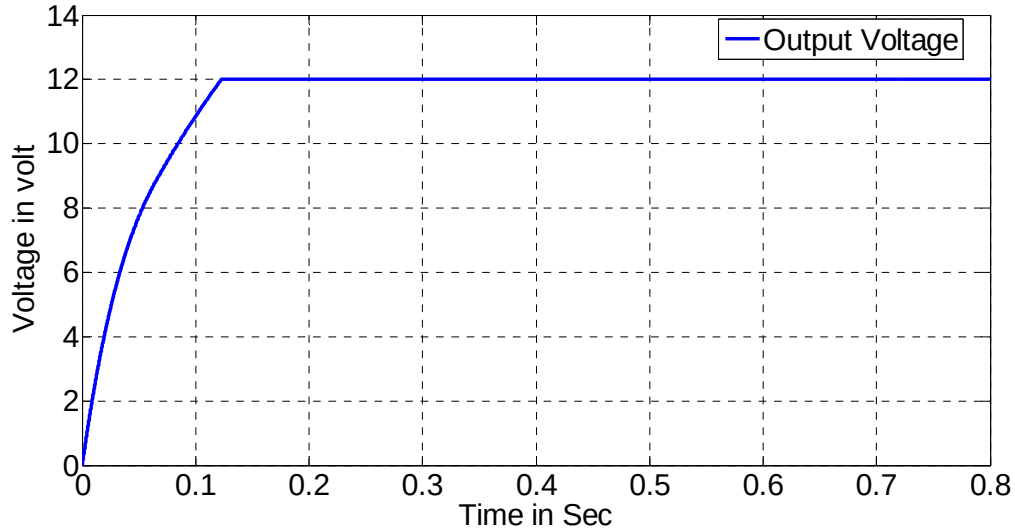


Figure 8. System response of output voltage of 12Volt

The waveforms in Figure 9 shows the system rated constant output current are measured under the input voltage 10volts to 16 volts it gives constant 3Amps. Figure 10 shows the system output power in watts it gives 36watts. It can be shows that the proposed buck–boost converter can operate stably in CCM for any load under the closed-loop control.

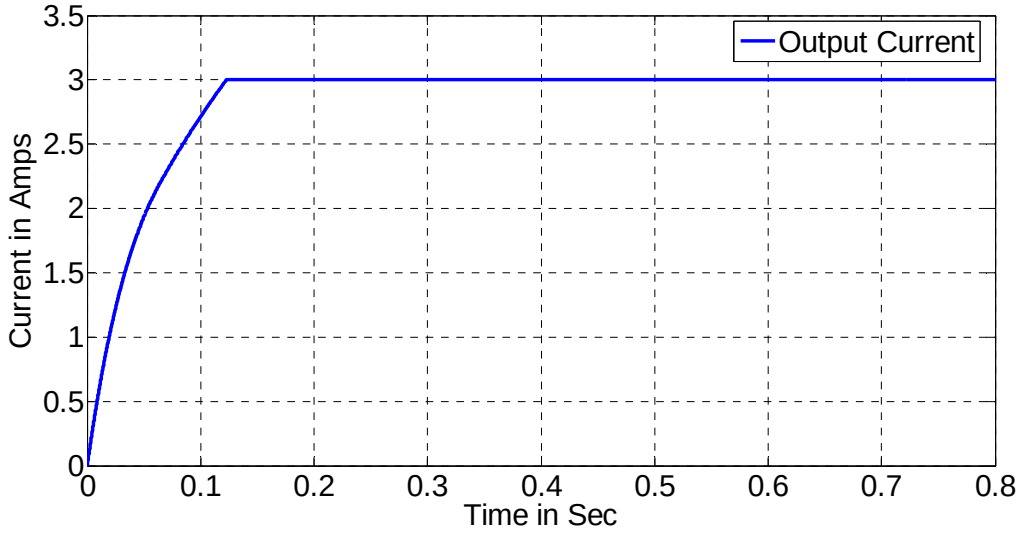


Figure 9. System response of output current 3Amps

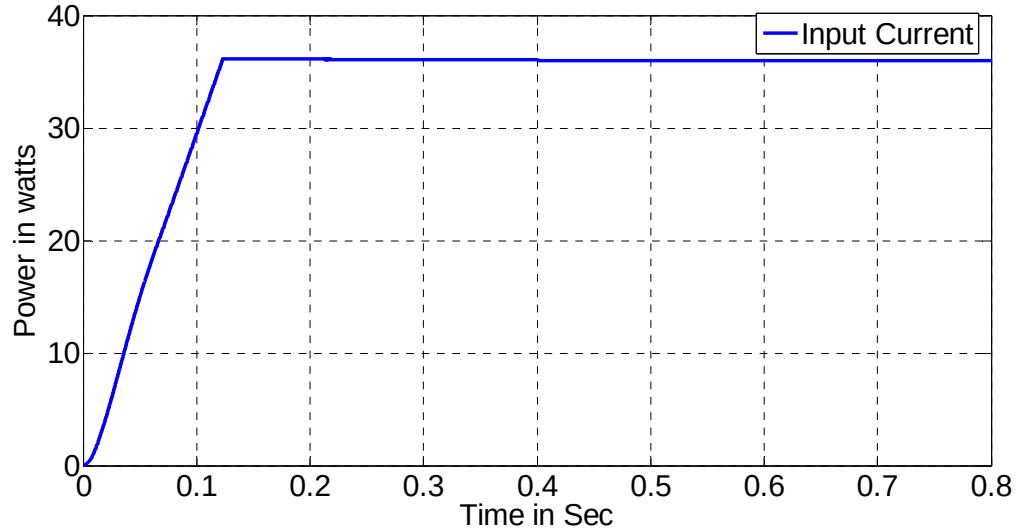
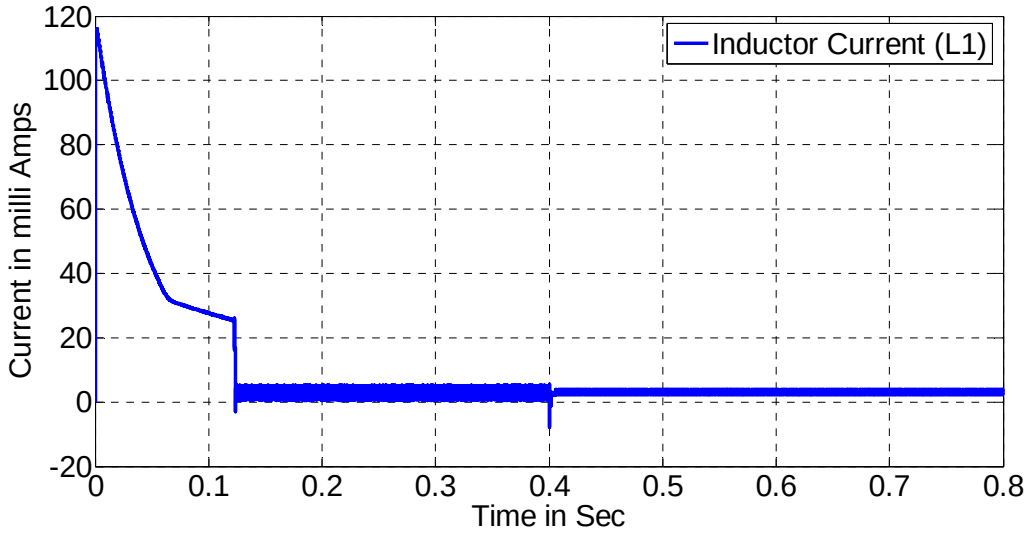
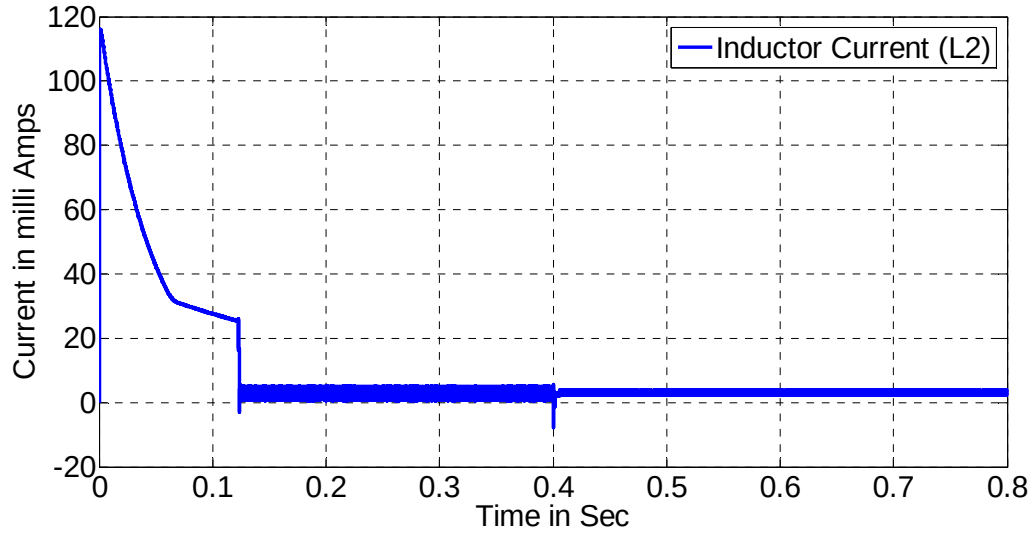


Figure 10. System output power

The wavefrom Figure 11(a) and (b) shows the system inductor current, during 0 to 0.4 sec the system start bucking condition because of the input voltage is 16volt and the time period of duty cycle D is less then the 1-D shown in Figure 12 (a) and during 0.4 to 0.8 sec the system start boosting because of the input voltage is less the system output voltage i.e. 12volts at that time period the duty cycle D is greater than the 1-D shown in Figure 12 (b).

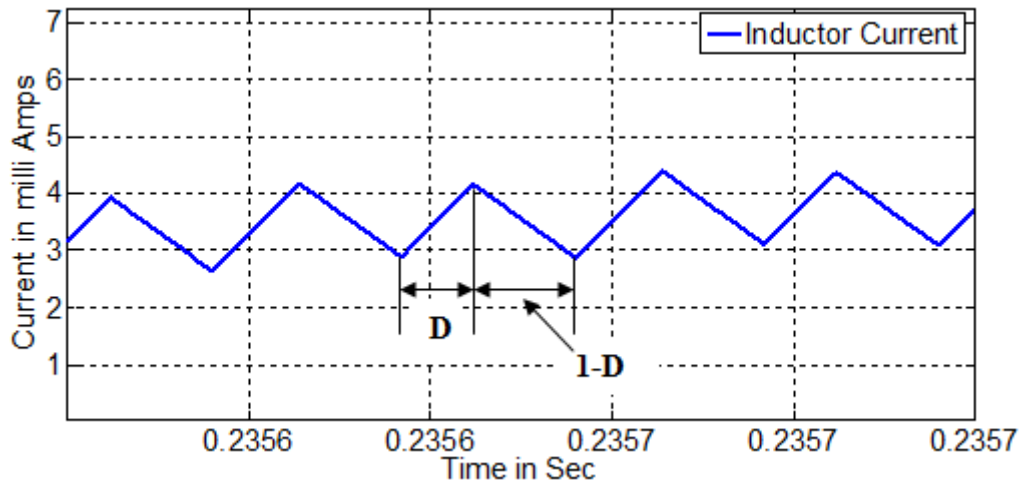


(a)

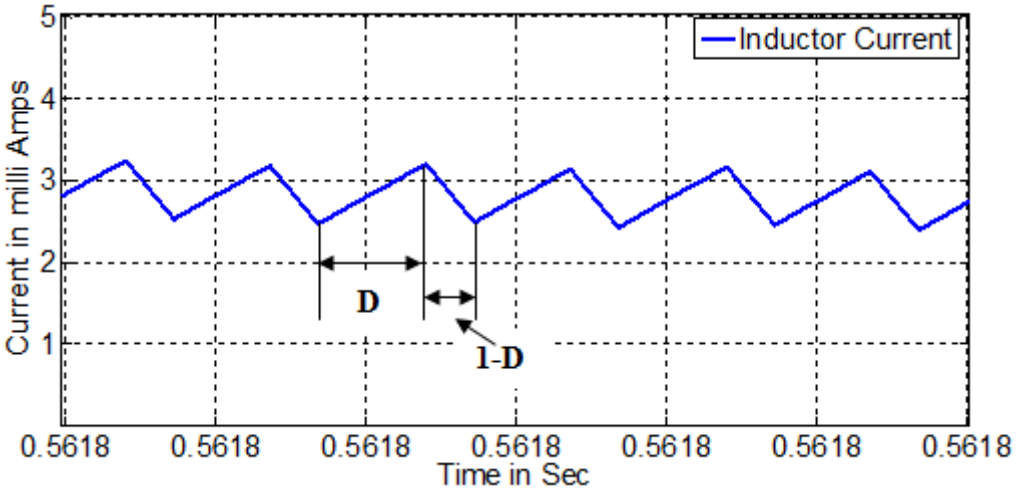


(b)

Figure 11. Inductor current (a) L_1 (b) L_2



(a)



(b)

Figure 12. Zoom wavefrom for inductor current (a) Bucking condtion (b) Boosting condition

8. CONCLUSION

The proposed buck–boost converter, combining the 1-plus-D converter and the SR buck by using the same power switches, has a positive output voltage and no right-half plane zero. Furthermore, this converter always operates inCCM inherently, thereby causing variations in duty cycle all over the load range not to be so much, and hence, the control of the converter to be easy. Above all, such a converter possesses the nonpulsating output current, thereby not only decreasing the current stress on the output capacitor but also reducing the output voltage ripple. By means of experimental results, it can be seen that for any input voltage, the proposed converter can stably work for any dc load current; with the output voltage 12V was controlled accurately.

REFERENCES

[1] R.W. Erickson and D. Maksimovic, Fundamentals of Power Electronics, 2nd ed. Norwell, MA, Kluwer, 2001.
[2] N. Mohan, T.M. Undeland, and W.P. Robbins, Power Electronics, 2nd ed. New York: Willey, 2003.
[3] F.L. Luo, "Positive output Luo converters: Voltage lift technique", IEEE Proc. Elect. Power Appl., vol. 4, no. 146, pp. 415–432, Jul. 1999.
[4] X. Chen, F.L. Luo, and H. Ye, "Modified positive output Luo converter", in Proc. IEEE Int. Conf. Power Electron. Drive Syst., 1999, pp. 450–455.
[5] F.L. Luo and H. Ye, "Positive output super-lift converters", IEEE Trans. Power Electron, vol. 18, no. 1, pp. 105–113, Jan. 2003.
[6] F.L. Luo and H. Ye, "Positive output multiple-lift push-pull switchedcapacitor Luo-converters", IEEE Trans. Ind. Electron, vol. 51, no. 3, pp. 594–602, Jun. 2004.
[7] M. Zhu and F.L. Luo, "Development of voltage lift technique on doubleoutput transformerless DC–DC converter", in Proc. 33rd Annu Conf. Ind. Electron. Soc., 2007, pp. 1983–1988.
[8] M. Zhu and L. Luo, "Implementing of developed voltage lift technique on SEPIC, Cuk and double-output DC–DC converters", in Proc. IEEE Int. Conf. Ind. Electron., 2007, pp. 674–681.
[9] K. Viswanathan, D. Srinivasan, and R. Oruganti, "A universal fuzzy controller for a non-linear power electronic converter", in Proc. IEEE Int. Conf. Fuzzy Syst., 2002, pp. 46–51.
[10] K.I. Hwu and Y.T. Yau, "Two types of KY buck–boost converters", IEEE Trans. Ind. Electron, vol. 56, no. 8, pp. 2970–2980, Aug. 2009.
[11] B. Axelrod, Y. Berkovich, and A. Ioinovici, "Hybrid switched-capacitor-Cuk/Zeta/Sepic converters in step-up mode", Proc. IEEE Int. Symp. Circuits Syst., pp. 1310–1313, 2005.
[12] Jeevan Naik, "Synchronous Buck-Boost Converter for Energy Harvesting Application", IJERT, ISSN: 2278-0181, Vol. 3 Issue 6, June - 2014, pp. 908-912.

BIOGRAPHY OF AUTHOR

Jeevan Naik was born in Karwar, Karnataka, India, in 1987. He received the Diploma degree in Electrical and Electronic Engineering from Department Of Technical Education, Bangalore, Karnataka, India in 2008 and B.E degree in Electrical and Electronic Engineering from Visvesvaraya Technological University, Belgaum, Karnataka, India in 2011. He received the M.Tech degree in power electronic from the Visvesvaraya Technological University, Belgaum, Karnataka, India in 2013.

His current research interests include Modeling, Simulation and Control of HVDC and Power Electronics Converter using MATLAB/SIMULINK and PSpice and also intersert in Matrix Converters, Active & Hybrid Filters, SMPS design and development, Application of Power Electronics in Renewable EnergySystems and Electrified Railway Systems, Reactive Power Control, Harmonics and Power Quality Compensation Systems such as SVC, UPQC and FACTS devices. Since 2013, he is now Project Engineer in CSIR - National Aerospace Laboratories, Bangalore, Karnataka, India. Has been a member of the Iran Elites National Foundation. He isthe author of more than 20 journal and conference papers. Also, he is a reviewer and Editorial Board member of several international journals.